A Fully Monolithic SiGe Quadrature Voltage Controlled Oscillator Design for GSM/DCS-PCS Applications

David Cordeau[1,2], Jean-Marie Paillot[2], Hervé Cam[1], Giuseppe De Astis[1], Lucian Dascalescu[2]

[1]ACCO, 21 bis rue d'Hennemont, 78100 Saint-Germain-en-Laye, France
[2]LAII-ESIP,UPRES_EA 1219, IUT d'Angoulême- 4, avenue de Varsovie 16021 Angoulême, France

Abstract — **This paper describes the design and optimization in terms of phase noise of a fully monolithic SiGe Voltage Controlled Oscillator (VCO) with quadrature outputs. The proposed circuit is made of two cross-coupled differential VCO's, with integrated resonator, to ensure the quadrature outputs. The quadrature VCO core runs on 13 mA from a 2.7 V power supply. The simulated phase noise is about –140 dBc/Hz at 3 MHz frequency offset almost all over the tuning range. The oscillator is tuned from 1.44 GHz to 1.76 GHz with a tuning voltage varying from 0 to 3 V.**

I. INTRODUCTION

The remarkable growth in telecommunications systems, such as cellular telephony, demands continuous efforts toward the improvement of Radio-Frequency (RF) circuit performance. Concerning the Voltage Controlled Oscillators, the phase noise specifications become more and more restrictive with the appearance of new mobile phone generations. In the same way, communication systems become more and more complex and it clearly appears that the new communications architectures will need to use multi-phases frequency generators. For example, quadrature signals (0° and 90°) are required in zero-IF transceivers, in I/Q (de)modulators and in image rejection mixers. In common communication systems, phase accuracy is needed to ensure a right behaviour. Indeed, the carrier rejection and the transmission quality of any systems depend on the phase noise of the signals applied to the modulator. Therefore, it seems to be very interesting to combine minimum phase noise oscillator and quadrature signals generators design [1].

Due to this consideration, the present work aimed at designing an original low phase noise quadrature VCO, using SiGe HBT technology. This latter provides high output power [2] and good noise performance due to the low 1/f noise [3].

The present paper is organized into four sections. Section II treats the VCO design with three subsections concerning the phase noise minimization, the VCO core design and the design option choosen to generate the quadrature. Section III presents the simulation results followed by the conclusion in section IV.

II. VCO DESIGN

A. Phase Noise Minimization

By considering a simplistic model of an oscillator composed of a lossy resonator and a noiseless energy restorer, the expression of the noise (N) to signal (S) ratio is [4]:

$$\frac{N}{S}=\frac{\omega\cdot k\cdot T}{Q\cdot Pdiss} \qquad (1)$$

where ω is the angular center frequency, k the Boltzmann constant, T the temperature, Q the quality factor of the resonator and P_{diss} the dissipated power in the resistive parts of the resonator.

A more accurate expression for the phase noise of an oscillator was published by Leeson in 1966 [5]:

$$S\phi(f_m)=\left(\frac{f_0}{f_m}\right)^2\cdot\frac{F\cdot k\cdot T}{8\cdot Pdiss\cdot Q^2} \qquad (2)$$

where f_0 is the center frequency of oscillation, f_m the offset frequency and F the noise factor.

With these two expressions, it can be concluded that for a fixed loaded quality factor of the oscillator, the minimum phase noise is reached while maximizing the dissipated power in the resistive parts of the resonator which is related to the added power of the oscillator amplifier. An optimization of the transistor bias point, the current swing and the voltage swing (and consequently the dynamic load line of the amplifier) must be done in order to increase the added power of the amplifier. Thus, the design method consists in optimizing the dynamic load line so that a relatively high collector current swing and collector to emitter voltage swing could be seen across the transistor, without entering the saturation area of the active device.

B. VCO Core Design

The quadrature VCO core uses a differential VCO structure as shown in Fig. 1.

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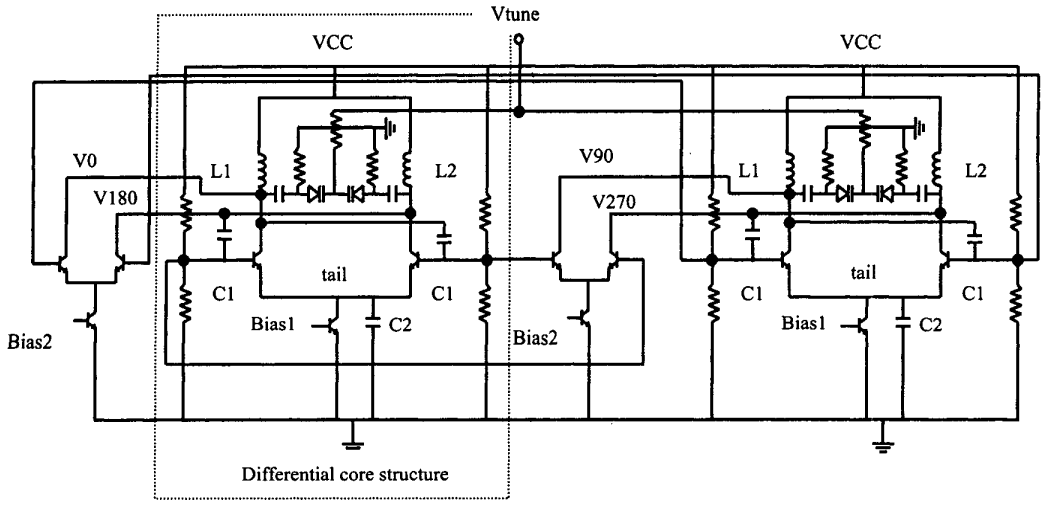

Fig.1. Quadrature VCO schematic

The feedback of the VCO is performed by a capacitive cross-coupling of the collector and base terminals of the differential pair. The frequency of oscillation is determined by the LC parallel resonator at the collectors. The tuning range depends on the global capacitance C variation and thus on the C_{max}/C_{min} ratio of the varactor diodes and on the AC coupling capacitor. The two inductors L1 and L2 are coupled in order to increase the inductance and the quality factor Q. The simulated Q of the structure, with Momentum software, is about 20 between 1.6 and 2.6 GHz. The capacitor C2 is a tail capacitor and is used to reduce phase noise due to the tail current source noise and to attenuate the voltage variations on the tail node. This latter effect results in more symmetric waveforms and smaller harmonic distortion in the output of the VCO [6].

To ensure proper startup of the oscillator, the following condition needs to be satisfied [7]:

$$\frac{g_m}{n} \cdot R_p > 1 \qquad (3)$$

where g_m is the small signal transconductance of the bipolar transistors, R_p the resistive parts of the resonator and n the ratio of collector to base voltage:

$$n = 1 + \frac{C_b}{C_1} \qquad (4)$$

where Cb is the input capacitance of the bipolar transistors.

According to (3), better startup conditions will be obtained with a low n value and a high small signal transconductance of the active device, which implies a relatively high tail current of the differential pair.

Fortunately, these two conditions also allow to obtain both a relatively high voltage swing across the resonator and a high collector current swing. Indeed, a low n value will force the circuit to oscillate with a relatively high collector and base voltage. In the same way, a relatively high g_m value ensures a better collector current swing. Consequently, better phase noise performance will be reached in this case, as shown in section II.*A*.

C. Quadrature Generation

Several design options are available to generate quadrature outputs such as, for example, the use of a VCO at double frequency followed by a divide by two divider.

The design option choosen here is similar to the one proposed in [1] where two CMOS differential VCO were cross-coupled.

The structure can easily be adapted to a bipolar SiGe technology as shown in Fig. 1.

Of course, this option comes at the cost of double VCO area and consumption, but it provides relatively high voltage swing and can consequently directly drive the image rejection mixer or other circuits connected to it.

III. Simulations Results

The simulations results presented in this section were obtained with the Agilent's software ADS.

With a 6 mA core current VCO (for one differential VCO) and a n parameter of about 1.3, the dynamic load line of the active part of the VCO is as shown in Fig. 2.

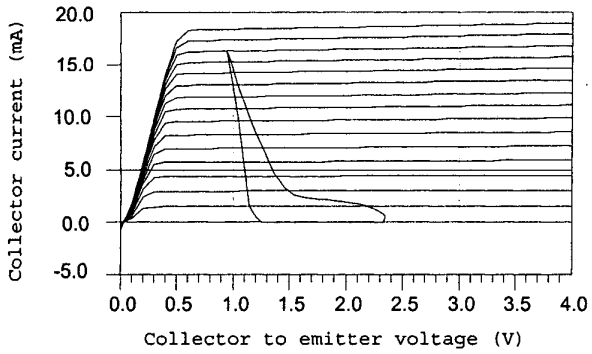

Fig.2. Dynamic load line of the active part of the VCO for a tuning voltage of 1.5 V.

One can argue that the collector to emitter voltage swing and the collector current swing are not as high as they could be. Nevertheless, this dynamic load line is at its optimum for the VCO topology and the technology used.

Consequently, the phase noise is at its optimum and its simulated value versus the tuning voltage is plotted on Fig. 3. As shown on this figure, the VCO phase noise level is close to –140 dBc/Hz at 3 MHz frequency offset almost all over the tuning range, slightly worse close to 0V tuning voltage because of the high non linearity of the varactors diodes in this area of operation.

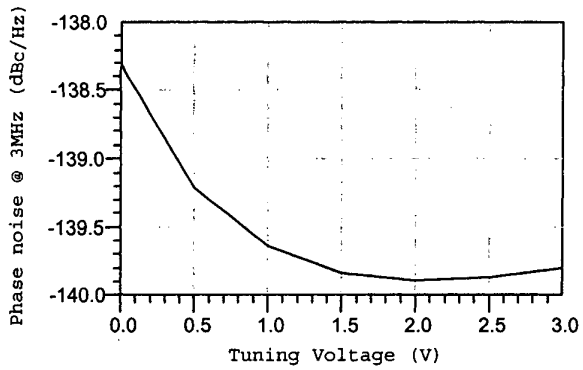

Fig.3. Simulated phase noise of the quadrature VCO versus the tuning range.

As shown in Fig. 4, the tuning range of the VCO is about 320 MHz but better range could be reached, if desired, by re-sizing the varactor area and reducing the AC coupling capacitor of the two differential VCO.

Emitter follower are used on each output in order to improve the pulling performance of the quadrature VCO. Two adders with LC networks are employed in order to adjust the quadrature at the outputs and to match the 50 Ω loads.

The simulated output spectrum on 50Ωload is shown in Fig. 5 for a tuning voltage of 1.5V and the four outputs of the quadrature VCO are plotted on Fig. 6.

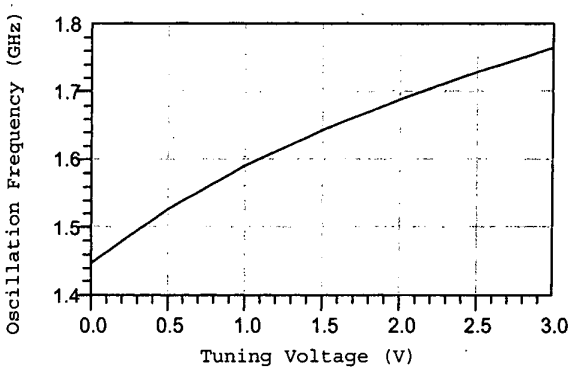

Fig.4. Tuning characteristic of the quadrature VCO.

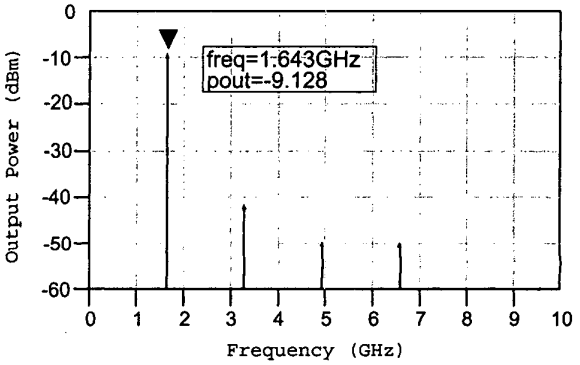

Fig.5. Simulated output spectrum of the VCO.

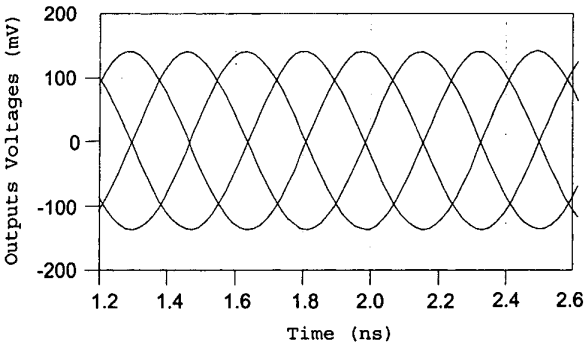

Fig.6. Output Quadrature Waveforms of the VCO.

The simulated output power is about –9 dBm on 50 Ω load and Fig. 6 shows a good quadrature at the output of the VCO.

The simulation performances of this SiGe quadrature VCO are summarized in Table I and Fig. 7 shows the layout of the circuit.

TABLE I
SUMMARY OF QUADRATURE VCO SIMULATED PERFORMANCES

Supply Voltage (V)	2.7
DC Current Consumption (mA) (without buffers)	13
Phase Noise @ 3MHz (dBc/Hz) (In the middle of the band)	-139.8
Output Power (dBm) (50Ωload)	-9
Tuning Range (MHz)	320
Tuning Voltage (V)	0-3

IV. CONCLUSION

A fully monolithic SiGe quadrature VCO prototype at 1.6 GHz is presented in this paper. A phase noise minimization technique was applied to the design of the differential VCO structures. A tuning range of about 320 MHz is obtained in simulation and a simulated phase noise of about –140 dBc/Hz at 3 MHz frequency offset was found under a 2.7 V power supply with a 13mA DC current.

The simulation results are very encouraging. By using a low cost, low noise technology such as a bipolar SiGe technology, this circuit could find its place in a GSM/DCS-PCS transceiver. A prototype is being processed and will be tested by the end of the first semester of 2002.

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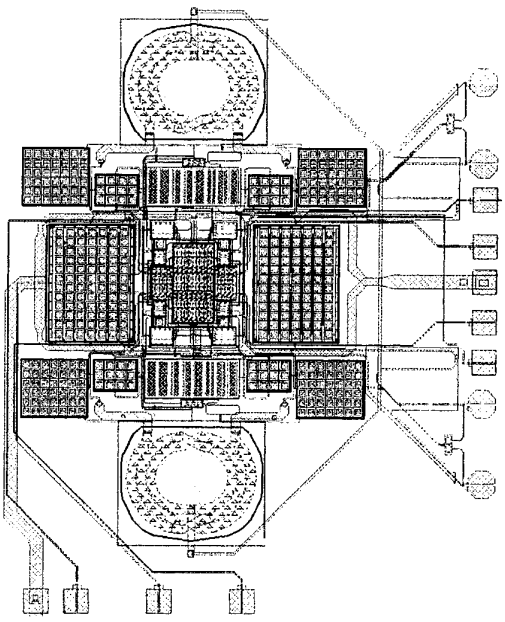

Fig.7. Layout of the SiGe Quadrature VCO

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